

Fast Logic Solver Test-bench - User story #811

Clean-up of probe vhdl code

22.04.2021 19:13 - Katarina Cindric

Status:	Closed	Start date:	22.04.2021
Priority:	Normal	Due date:	
Assignee:	Pedro Lourenco	% Done:	0%
Category:		Estimated time:	0.00 hour
Target version:	Test-bench for PLC interface v0.1.0	Spent time:	0.00 hour
Git branch (link):		SVN commit (link/?p=rev):	
Git merge to develop (link):			
Description			
Clean-up of probe vhdl code			

History

#1 - 22.04.2021 19:16 - Katarina Cindric

- Status changed from New to Code: Impl

#2 - 05.05.2021 08:33 - Katarina Cindric

- Target version set to Test-bench for PLC interface v0.1.0

#3 - 11.05.2021 17:28 - Katarina Cindric

- Status changed from Code: Impl to Closed