Fast Logic Solver Test-bench - User story #812

Test UART in ISE in loop-back form

22.04.2021 19:14 - Katarina Cindric

Status:	Closed	**Start date:**	22.04.2021
Priority:	Normal	**Due date:**	
Assignee:	Katarina Cindric	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	Test-bench for PLC interface v0.1.0	**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

Test UART in ISE in loop-back form

History

#1 - 05.05.2021 08:29 - Katarina Cindric

- Assignee deleted (Pedro Lourenco)

#2 - 05.05.2021 08:34 - Katarina Cindric

- Target version set to Test-bench for PLC interface v0.1.0

#3 - 05.05.2021 08:34 - Katarina Cindric

- Status changed from New to Code: Impl

#4 - 11.05.2021 17:35 - Katarina Cindric

- Assignee set to Pedro Lourenco

#5 - 02.06.2021 08:32 - Katarina Cindric

- Status changed from Code: Impl to Unit: Rev

#6 - 15.06.2021 20:13 - Pedro Lourenco

The UART module developed was successfully tested using VHDL test benches in ISE with ISIM. These are currently being migrated to VUNIT + ModelSim. The current UART version, also used in the LabView FPGA projects, can be found at [[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/blob/42694fba4bc84a3a823b0f58f65a51de38489125/Firmware/Xilinx/FLSTestBench/hdl/source/uart/lv_uart_wrapper.vhd]].

#7 - 29.06.2021 17:42 - Katarina Cindric

- Assignee changed from Pedro Lourenco to Katarina Cindric

#8 - 29.06.2021 17:44 - Katarina Cindric

- Status changed from Unit: Rev to Closed