Fast Logic Solver Test-bench - User story #813

Test pulse/probe in ISE in loopback mode

22.04.2021 19:14 - Katarina Cindric

Status:	Arch: Rev	**Start date:**	22.04.2021
Priority:	Normal	**Due date:**	
Assignee:		**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:		**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

Test pulse/probe in ISE in loopback mode

History

#1 - 05.05.2021 08:30 - Katarina Cindric

- Assignee deleted (Pedro Lourenco)

#2 - 05.05.2021 08:34 - Katarina Cindric

- Target version set to Test-bench for PLC interface v0.1.0

#3 - 05.05.2021 08:34 - Katarina Cindric

- Status changed from New to Arch: Rev

#4 - 05.05.2021 08:34 - Katarina Cindric

- Status changed from Arch: Rev to Code: Impl

#5 - 11.05.2021 17:45 - Katarina Cindric

- Target version deleted (Test-bench for PLC interface v0.1.0)

#6 - 11.05.2021 17:45 - Katarina Cindric

- Status changed from Code: Impl to New

#7 - 30.11.2021 09:30 - Katarina Cindric

- Status changed from New to Arch: Rev

#8 - 30.11.2021 22:46 - Pedro Lourenco

Objective of testing the Pulse Generator and Pulse Probe components successfuly implemented. However, the two components were tested and validated individually with VHDL test benches oscilloscope measurements. For additional information see the following README.md files:

- Pulse Generator - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/blob/plc_interface_v0.3.0/Firmware/Xilinx/PulseGenerator/README.md
- Pulse Probe - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/blob/plc_interface_v0.3.0/Firmware/Xilinx/PulseProbe/README.md