# Fast Logic Solver Test-bench - User story #815

## Migrate signal generator to Labview

22.04.2021 19:15 - Katarina Cindric

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|---|---|---|---|
| **Status:** | Unit: Rev | **Start date:** | 22.04.2021 |
| **Priority:** | Normal | **Due date:** | |
| **Assignee:** | Katarina Cindric | **% Done:** | 0% |
| **Category:** | | **Estimated time:** | 0.00 hour |
| **Target version:** | | **Spent time:** | 0.00 hour |
| **Git branch (link):** | | **SVN commit (link/?p=rev):** | |
| **Git merge to develop (link):** | | | |

**Description**

Migrate signal generator to Labview

### History

**#1 - 05.05.2021 08:29 - Katarina Cindric**

*- Assignee deleted (Pedro Lourenco)*

**#2 - 02.09.2021 15:14 - Pedro Lourenco**

Signal generator (InputEmulator) successfully deployed in Labview and already in use for FLSTestBench InputStage tests.
Please see the following links:

- Source Code - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/tree/fls_v0.4.1/Firmware/Xilinx/PulseGenerator
- LabView FPGA Project - https://vcis-svn.f4e.europa.eu/svn/52EC-FLS/tags/fls_v0.4.1/LabViewFPGA/FLSTestBenchFirmwares/NI9157__Tag_Fls_v0_4_1__InputStage
- FLSTestBench FLSInterface - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/blob/fls_v0.4.1/Software/MARTe2/Source/Components/Interfaces/FLSInterface/FLSInterface.h
- FLSTestBench FlsInputStageTests - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/blob/fls_v0.4.1/Software/MARTe2/Test/IntegrationTests/FlsInputStage/FlsInputStageTest.h

**#3 - 30.11.2021 09:26 - Katarina Cindric**

*- Status changed from New to Arch: Rev*

**#4 - 30.11.2021 09:26 - Katarina Cindric**

*- Status changed from Arch: Rev to Unit: Rev*

**#5 - 30.11.2021 09:26 - Katarina Cindric**

*- Assignee set to Katarina Cindric*