Fast Logic Solver Test-bench - User story #816

Migrate probe to Labview

22.04.2021 19:15 - Katarina Cindric

Status:	Unit: Rev	**Start date:**	22.04.2021
Priority:	Normal	**Due date:**	
Assignee:	Katarina Cindric	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:		**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

Migrate probe to Labview

History

#1 - 05.05.2021 08:30 - Katarina Cindric

- Assignee deleted (Pedro Lourenco)

#2 - 05.10.2021 19:14 - Pedro Lourenco

The VHDL Module Pulse Probe (a.k.a Output Detector) been successfully developed, tested and migrated into LabView FPGA, currently being used in the FLSTestBench Tests for release/tag v0.7.x. Please find additional information here:

- Commit Tag - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/commit/6d37d240423e5d9b5bd08676912088f6be6f9daf
- Source Code - https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/tree/master/Firmware/Xilinx/PulseProbe
- LabView Deployment - https://vcis-svn.f4e.europa.eu/svn/52EC-FLS/tags/fls_v0.7.0/LabViewFPGA/FLSTestBenchFirmwares/NI9157__Tag_Fls_v0_7_0__OutputStage/output_detector/

#3 - 30.11.2021 09:26 - Katarina Cindric

- Status changed from New to Arch: Rev

#4 - 30.11.2021 09:26 - Katarina Cindric

- Status changed from Arch: Rev to Unit: Rev

#5 - 30.11.2021 09:26 - Katarina Cindric

- Assignee set to Katarina Cindric