Fast Logic Solver Test-bench - User story #844

Unit test automation

11.05.2021 17:30 - Katarina Cindric

Status:	Unit: Rev	**Start date:**	11.05.2021
Priority:	Normal	**Due date:**	
Assignee:	Pedro Lourenco	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	Test-bench for PLC interface v0.1.0	**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

Look for a way to automatize the execution of multiple unit tests of a unit under test, e.g. probe.

History

#1 - 11.05.2021 17:30 - Katarina Cindric

- Status changed from New to Code: Impl

#2 - 15.06.2021 18:17 - Katarina Cindric

- Status changed from Code: Impl to Unit: Rev

#3 - 15.06.2021 20:39 - Pedro Lourenco

VHDL unit tests were automated using VUNIT as displayed here: [[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/commit/f8e319bc32b814f04e4c288b7d214bfc1b1e0b2e]]