Fast Logic Solver Test-bench - User story #845

Loopback UART test with C code and Labview

11.05.2021 17:47 - Katarina Cindric

Status:	Closed	**Start date:**	11.05.2021
Priority:	Normal	**Due date:**	
Assignee:	Katarina Cindric	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	Test-bench for PLC interface v0.1.0	**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

Test UART block in Labview using the simple C code app. Connect RX to TX and write and read from the module using the simple application

History

#1 - 11.05.2021 17:47 - Katarina Cindric

- Status changed from New to Code: Impl

#2 - 02.06.2021 08:32 - Katarina Cindric

- Status changed from Code: Impl to Unit: Rev

#3 - 15.06.2021 20:22 - Pedro Lourenco

UART successfully tested in loop back using with the LabView C API based test code and LabView FPGA firmware.
[[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/commit/61c03be7b73762ec8ef0cc0027556793068a76e4]]

#4 - 29.06.2021 17:43 - Katarina Cindric

- Assignee changed from Pedro Lourenco to Katarina Cindric

#5 - 29.06.2021 17:45 - Katarina Cindric

- Status changed from Unit: Rev to Closed