Fast Logic Solver Test-bench - User story #867

PLC interface integrated test with MARTe2 app

02.06.2021 08:29 - Katarina Cindric

Status:	Closed	**Start date:**	02.06.2021
Priority:	Normal	**Due date:**	
Assignee:	Pedro Lourenco	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	Test-bench for PLC interface v0.1.0	**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

History

#1 - 02.06.2021 08:29 - Katarina Cindric

- Status changed from New to Code: Impl

#2 - 15.06.2021 18:14 - Katarina Cindric

- Status changed from Code: Impl to Unit: Rev

#3 - 15.06.2021 18:18 - Katarina Cindric

- Status changed from Unit: Rev to Unit: Impl

#4 - 15.06.2021 18:18 - Katarina Cindric

- Status changed from Unit: Impl to Unit: Rev

#5 - 15.06.2021 20:42 - Pedro Lourenco

Migrated the simple C application used to test the UART loopback firmware into MARTe2 GTests: [[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/commit/e9963c2429d4303c989e1a20ce10020d434fafbc]] .

#6 - 29.06.2021 17:44 - Katarina Cindric

- Status changed from Unit: Rev to Closed