# Fast Logic Solver Test-bench - User story #880

## PLC interface v0.1.0 integrated test with MARTe2 app

15.06.2021 18:21 - Katarina Cindric

| | | | |
|---|---|---|---|
| **Status:** | Closed | **Start date:** | 15.06.2021 |
| **Priority:** | Normal | **Due date:** | |
| **Assignee:** | Pedro Lourenco | **% Done:** | 0% |
| **Category:** | | **Estimated time:** | 0.00 hour |
| **Target version:** | Test-bench for PLC interface v0.1.0 | **Spent time:** | 0.00 hour |
| **Git branch (link):** | | **SVN commit (link/?p=rev):** | |
| **Git merge to develop (link):** | | | |

**Description**

Test PLC interface v0.1.0 in Labview

### History

**#1 - 15.06.2021 18:21 - Katarina Cindric**

*- Status changed from New to Arch: Rev*

**#2 - 15.06.2021 18:21 - Katarina Cindric**

*- Status changed from Arch: Rev to 13*

**#3 - 15.06.2021 18:22 - Katarina Cindric**

*- Status changed from 13 to Unit: Rev*

**#4 - 15.06.2021 20:33 - Pedro Lourenco**

Released FLSTestBench tag 'plc_interface_v0.1.0' corresponding to the sucessful testing of FLS tag 'plc_interface_v0.1.0'.

[[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/tags/plc_interface_v0.1.0]]

```
<?xml version="1.0" encoding="UTF-8"?>
<testsuites tests="28" failures="0" disabled="0" errors="0" timestamp="2021-06-11T14:47:45" time="1.242" name=
"AllTests">
  <testsuite name="FlsPlcInterfaceGTest" tests="28" failures="0" disabled="0" errors="0" time="1.241">
    <testcase name="TestHelperConstructor" status="run" time="0" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4r" status="run" time="0.222" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4r4r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1w4r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4w4r4w" status="run" time="0.013" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r3w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_2r2w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_3r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r2w1r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r1r1r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl0ms_1m3r" status="run" time="0.013" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r1m2r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_2r1m1r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_3r1m" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_2r1rp2r" status="run" time="0.012" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5ms_4r" status="run" time="0.027" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl5ms_4r4r" status="run" time="0.047" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl30ms_4r" status="run" time="0.102" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl39ms_4r" status="run" time="0.132" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl40ms_4r" status="run" time="0.132" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl5_10_10ms_4r" status="run" time="0.037" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl39_5_5ms_4r" status="run" time="0.062" classname="FlsPlcInterfaceGTest"
/>
```

```
    <testcase name="TestUartLoop_chdl40_5_5ms_4r" status="run" time="0.062" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_39_5ms_4r" status="run" time="0.061" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_40_5ms_4r" status="run" time="0.063" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_5_39ms_4r" status="run" time="0.061" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_5_40ms_4r" status="run" time="0.063" classname="FlsPlcInterfaceGTest"
/>
  </testsuite>
</testsuites>
```

**#5 - 29.06.2021 17:46 - Katarina Cindric**

*- Status changed from Unit: Rev to Closed*