Fast Logic Solver Test-bench - User story #881

Test FLS v0.1.0 against FLS test bench with the test cases

15.06.2021 18:30 - Katarina Cindric

Status:	Closed	**Start date:**	15.06.2021
Priority:	Normal	**Due date:**	
Assignee:	Katarina Cindric	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	Test bench for FLS v0.1.0	**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

- write and read to and from a register (with and without increment combinations)

History

#1 - 15.06.2021 18:30 - Katarina Cindric

- Status changed from New to Arch: Rev

#2 - 15.06.2021 21:07 - Pedro Lourenco

Test for FLS tag 'fls v0.1.0' implemented in MARTe2: [[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/commit/5091f566f02506d14124dca7bd13eb8a2420c9de]] .
The corresponding tag 'fls v0.1.0' for the FLSTestBench was not released as 3 of the tested cases failed:

```
<?xml version="1.0" encoding="UTF-8"?>
<testsuites tests="52" failures="3" disabled="0" errors="0" timestamp="2021-06-11T17:43:26" time="1.783" name=
"AllTests">
  <testsuite name="FlsRegisterManagerGTest" tests="24" failures="3" disabled="0" errors="0" time="0.543">
    <testcase name="TestHelperConstructor" status="run" time="0.001" classname="FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_StAddr" status="run" time="0.22" classname="FlsRegisterManagerGTest
" />
    <testcase name="TestRegisterLoop_Addr0_SetAddrInvalid" status="run" time="0.012" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_RdAddr" status="run" time="0.012" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_StInvalidRdAddr" status="run" time="0.013" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_StRdAddr" status="run" time="0.013" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_Wr" status="run" time="0.013" classname="FlsRegisterManagerGTest"
/>
    <testcase name="TestRegisterLoop_Addr0_Rd" status="run" time="0.013" classname="FlsRegisterManagerGTest"
/>
    <testcase name="TestRegisterLoop_Addr0_WrRd" status="run" time="0.015" classname="FlsRegisterManagerGTest"
 />
    <testcase name="TestRegisterLoop_Addr0_RdWr" status="run" time="0.014" classname="FlsRegisterManagerGTest"
 />
    <testcase name="TestRegisterLoop_Addr0_WrInc" status="run" time="0.014" classname="FlsRegisterManagerGTest
" />
    <testcase name="TestRegisterLoop_Addr0_RdInc" status="run" time="0.014" classname="FlsRegisterManagerGTest
" />
    <testcase name="TestRegisterLoop_Addr0_WrIncRdInc" status="run" time="0.016" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_RdIncWrInc" status="run" time="0.017" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_WrIncWr" status="run" time="0.016" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_WrIncRd" status="run" time="0.016" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_WrWrInc" status="run" time="0.015" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_WrRdInc" status="run" time="0.016" classname="
FlsRegisterManagerGTest" />
```

```
    <testcase name="TestRegisterLoop_Addr0_RdIncWr" status="run" time="0.016" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_RdIncRd" status="run" time="0.016" classname="
FlsRegisterManagerGTest">
      <failure message="FlsRegisterManagerGTest.cpp:380&#x0A;Value of: ret&#x0A;  Actual: false&#x0A;
Expected: true" type=""><![CDATA[FlsRegisterManagerGTest.cpp:380
Value of: ret
  Actual: false
Expected: true]]></failure>
    </testcase>
    <testcase name="TestRegisterLoop_Addr0_RdWrInc" status="run" time="0.016" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_RdRdInc" status="run" time="0.015" classname="
FlsRegisterManagerGTest" />
    <testcase name="TestRegisterLoop_Addr0_CmdsWithReplyBit_0x0000" status="run" time="0.014" classname="
FlsRegisterManagerGTest">
      <failure message="FlsRegisterManagerGTest.cpp:431&#x0A;Value of: ret&#x0A;  Actual: false&#x0A;
Expected: true" type=""><![CDATA[FlsRegisterManagerGTest.cpp:431
Value of: ret
  Actual: false
Expected: true]]></failure>
    </testcase>
    <testcase name="TestRegisterLoop_Addr0_CmdsWithReplyBit_0xF0F0" status="run" time="0.016" classname="
FlsRegisterManagerGTest">
      <failure message="FlsRegisterManagerGTest.cpp:448&#x0A;Value of: ret&#x0A;  Actual: false&#x0A;
Expected: true" type=""><![CDATA[FlsRegisterManagerGTest.cpp:448
Value of: ret
  Actual: false
Expected: true]]></failure>
    </testcase>
  </testsuite>
  <testsuite name="FlsPlcInterfaceGTest" tests="28" failures="0" disabled="0" errors="0" time="1.24">
    <testcase name="TestHelperConstructor" status="run" time="0.001" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4r" status="run" time="0.22" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4r4r" status="run" time="0.013" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1w4r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4w4r4w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r3w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_2r2w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_3r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_4r1w" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r2w1r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r1r1r1w" status="run" time="0.013" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl0ms_1m3r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_1r1m2r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_2r1m1r" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_3r1m" status="run" time="0.012" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl0ms_2r1rp2r" status="run" time="0.012" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5ms_4r" status="run" time="0.027" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl5ms_4r4r" status="run" time="0.047" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl30ms_4r" status="run" time="0.102" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl39ms_4r" status="run" time="0.132" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl40ms_4r" status="run" time="0.132" classname="FlsPlcInterfaceGTest" />
    <testcase name="TestUartLoop_chdl5_10_10ms_4r" status="run" time="0.037" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl39_5_5ms_4r" status="run" time="0.062" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl40_5_5ms_4r" status="run" time="0.062" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_39_5ms_4r" status="run" time="0.061" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_40_5ms_4r" status="run" time="0.063" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_5_39ms_4r" status="run" time="0.061" classname="FlsPlcInterfaceGTest"
/>
    <testcase name="TestUartLoop_chdl5_5_40ms_4r" status="run" time="0.063" classname="FlsPlcInterfaceGTest"
/>
  </testsuite>
</testsuites>
```


#3 - 29.06.2021 17:42 - Katarina Cindric

- Status changed from Arch: Rev to Unit: Rev

#4 - 29.06.2021 17:42 - Katarina Cindric

- Assignee changed from Pedro Lourenco to Katarina Cindric

#5 - 28.07.2021 14:08 - Katarina Cindric

- Status changed from Unit: Rev to Closed