Fast Logic Solver Test-bench - User story #894

Develop FLS v0.3.0 test bench

29.06.2021 17:50 - Katarina Cindric

Status:	Closed	**Start date:**	29.06.2021
Priority:	Normal	**Due date:**	
Assignee:	Katarina Cindric	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:	Test bench for FLS v0.3.0	**Spent time:**	0.00 hour
Git branch (link):		**SVN commit (link/?p=rev):**	
Git merge to develop (link):			

Description

Develop test bench to test the full register map of the FLS

History

#1 - 29.06.2021 17:51 - Katarina Cindric

- Status changed from New to Arch: Rev

#2 - 09.07.2021 13:43 - Pedro Lourenco

FLSTestBench v0.3.0 successfully implemented for handling fw tags *fls_0.3.x*.
Please find the source code here: [[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/commit/3d9cf6edb6e6aad9f365bb7d0c42cf832e16a370]].

#3 - 13.07.2021 16:23 - Katarina Cindric

- Assignee changed from Pedro Lourenco to Katarina Cindric

#4 - 13.07.2021 16:23 - Katarina Cindric

- Status changed from Arch: Rev to 13

#5 - 13.07.2021 16:23 - Katarina Cindric

- Status changed from 13 to Unit: Rev

#6 - 28.07.2021 14:10 - Katarina Cindric

- Status changed from Unit: Rev to Closed