# Fast Logic Solver Test-bench - User story #904

## Develop FLS v0.4.0 test bench

13.07.2021 16:27 - Katarina Cindric

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|---|---|---|---|
| **Status:** | Unit: Rev | **Start date:** | 13.07.2021 |
| **Priority:** | Normal | **Due date:** | |
| **Assignee:** | Katarina Cindric | **% Done:** | 0% |
| **Category:** | | **Estimated time:** | 0.00 hour |
| **Target version:** | Test bench for FLS v0.4.0 | **Spent time:** | 0.00 hour |
| **Git branch (link):** | | **SVN commit (link/?p=rev):** | |
| **Git merge to develop (link):** | | | |

**Description**

Develop test-bench to test the FLS v0.4.0

### History

**#1 - 13.07.2021 16:28 - Katarina Cindric**

*- Status changed from New to Arch: Rev*

**#2 - 23.07.2021 10:43 - Pedro Lourenco**

The FLSTestBench v0.4.x has been successfully implemented.

Key achievements (FLSInterface & FlsInputStage):

- Integration and configuration of the Input Emulator (Pulse Generator VHDL) methods for integrated testing;
- Write/Read the registers relevant for fls_v0.4.x testing using bit fields instead of full 16bit registers as a single words;
- Deployed the initial set of 50 tests, targeting the basic requirements funtionalities of the Input Stage (and Clock Generator);
- Additional tests will be added once this basic set is marked/accepted as PASS.

The source code can be found on branch *testbench_v04x* : [[https://vcis-gitlab.f4e.europa.eu/plourenco/flstestbench/-/tree/testbench_v04x]]

**#3 - 31.08.2021 17:37 - Katarina Cindric**

*- Status changed from Arch: Rev to Unit: Rev*

**#4 - 31.08.2021 17:39 - Katarina Cindric**

*- Assignee changed from Pedro Lourenco to Katarina Cindric*